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A Hawkins

PATENT APPLICATION

RESPONSE UNDER 37 CFR §1.116
EXPEDITED PROCEDURE
TECHNOLOGY CENTER ART UNIT 2834

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masayuki KIKUSHIMA

Application No.: 09/806,934

Filed: April 6, 2000

Group Art Unit: 2834

Examiner: M. Budd

Docket No.: 108574

For: PIEZOELECTRIC DEVICE AND METHOD FOR MANUFACTURING THE SAME

AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR §1.116

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

In reply to the Office Action mailed July 12, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 6 and 25 without prejudice to or disclaimer of the subject matter contained therein.

Please replace claims 1, 14, 22 and 26 as follows:

C1

1. (Twice Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit having a plurality of bumps formed thereon; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

C1 cancel'd.

the semiconductor integrated circuit being mounted in a center of an opening formed in a center of a base, and the semiconductor integrated circuit being connected to an input/output electrode pattern on the base through the plurality of bumps, and wherein the base includes a layered part, which surrounds the semiconductor integrated circuit, for mounting the piezoelectric resonator element, the layered part comprising at least two layers, including a first layer and a second layer, the first layer being below the second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

C2

14. (Twice Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

a plurality of bumps being formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit being mounted in an opening formed in a center of a base, and the semiconductor integrated circuit being connected to an input/output electrode pattern of the base through the plurality of bumps, and a protrusion being formed in at least one side wall of the base facing the side of the semiconductor integrated circuit and protruding into the opening to form the protrusion.

C3

22. (Twice Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

a plurality of bumps being formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit being mounted in a center of an opening formed in a center of a base, and the semiconductor

C3 amended. integrated circuit being connected to an input/output electrode pattern through the plurality of bumps by ultrasonic bonding, each of the plurality of bumps formed on the semiconductor integrated circuit being shaped to have two levels, a first level having a diameter 0.8 to 0.9 times and a second level having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

C4 26. (Twice Amended) The piezoelectric device according to claim 22, wherein the first level is 80 to 90 μm in diameter and 30 to 35 μm in height, and the second level is 40 to 45 μm in diameter and 30 to 35 μm in height.

REMARKS

Claims 1-5, 7-24 and 26-32 are pending herein, with claims 31 and 32 being withdrawn from consideration by way of a Restriction Requirement. By this Amendment, claims 1, 14, 22 and 26 are amended. In particular, claim 1 is amended to incorporate the subject matter of claim 6 therein, with claim 6 being correspondingly cancelled, claim 14 is amended to include the subject matter of claim 10 therein, claim 22 is amended to include the subject matter of claim 25 therein, with claim 25 being correspondingly cancelled, and claim 26 is amended to revise its dependency in view of the cancellation of claim 25. Claims 1, 14 and 22 are each amended to better define the invention in view of the prior art cited by the Examiner in the Office Action.

The attached Appendix includes a marked-up copy of the rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

Entry of this Amendment is proper under 37 CFR §1.116 since the Amendment (a) places the application in condition for allowance (for the reasons discussed herein), (b) does not raise any new issue requiring further search and/or consideration (since the amendments merely add previously considered dependent claims to the independent claims as explained above), (c) does not present any additional claims without canceling a corresponding number of

finally rejected claims, and (d) places the application in better form for appeal, should an appeal be necessary. The amendments are necessary and were not earlier presented because they are made in response to the position of the Patent Office taken in the Final Rejection. Entry of the Amendment is thus respectfully requested.

In view of the foregoing amendment and the following remarks, reconsideration of the application is respectfully requested.

I. Request for Approval of Drawing Corrections

Applicant again notes that a Request for Approval of Drawing Corrections was submitted with the Preliminary Amendment filed with the application on April 6, 2001. An additional courtesy copy of the Request for Approval of Drawing Correction is attached hereto for the convenience of the Patent Office. The Examiner is respectfully requested to indicate approval of the proposed drawing corrections in the next communication.

II. Rejection Under 35 U.S.C. §102(a)

Claims 1, 8, 9, 14, 20-24 and 27-30 were rejected under 35 U.S.C. §102(a) as allegedly being anticipated by JP -07-297666 (JP 666). This rejection is respectfully traversed.

The Patent Office relied upon Figure 4 in JP 666 in alleging that claims 1, 8, 9, 14, 20-24 and 27-30 were anticipated by JP 666.

However, JP 666 was not cited as teaching the features recited in dependent claims 6, 10 or 25. As claim 1 has been amended to include claim 6, claim 14 has been amended to include claim 10 and claim 22 has been amended to include claim 25, respectively, Applicant respectfully submits that this rejection has been overcome and should be withdrawn. Reconsideration and withdrawal of this rejection are respectfully requested.

III. Rejections Under 35 U.S.C. §103(a)

A. Kondo or Knecht in View of JP 732, JP 540 or JP 606

Claims 1-9 and 14-30 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 5,949,294 (Kondo) or U.S. Patent Nos. 5,405,476 (Knecht) in view of JP 04-18732 (JP 732), JP 08-264540 (JP 540) or JP 08-222606 (JP 606). This rejection is respectfully traversed.

First, as to claim 14, claim 14 has been amended to include the subject matter of claim 10, a claim not rejected based upon the cited references. As such, the rejection of claim 14 is overcome and should be withdrawn for this reason alone.

Second, as to claim 1, claim 1 now recites that the base of the device includes a layered part comprising at least two layers surrounding the semiconductor integrated circuit, and in which the opening of the first layer that is below a second layer is larger than the opening of the second layer. This embodiment is illustrated in, for example, Figure 9 of the present application. Neither Kondo nor Knecht teach or suggest a device having a base including such a layered part.

Kondo describes an oscillator formed from first and second containers, the first container including an integrated circuit active element 2 mounted therein and electrically connected to electrodes via wire bonding 12. A second, separate container 3 has an oscillating element 6 incorporated therein, and the second container 3 is attached onto an opening of the first container 1 so that electrodes of the respective containers are connected. By using separate containers, it is described that a damaged part may be easily removed and replaced without having to dispose of the entire unit. See the Abstract.

Knecht describes a particular method of mounting a piezoelectric element to a substrate using compliant conductive materials. As shown in Figure 2 of Knecht, the oscillator 100 includes an integrated circuit chip 104 mounted upon a substrate 106 and

connected to input-output pads via wire bonding. A piezoelectric element 102 is mounted upon ledges or sides 126 and 128 above the integrated circuit chip.

Knecht thus teaches the mounting of the integrated circuit upon a substrate with no layered parts at all. Kondo similarly describes that the integrated circuit is mounted upon a substrate without layered parts.

None of JP 732, JP 540 or JP 606 remedy the deficiencies of Kondo and Knecht in this regard. The Patent Office relied upon these secondary Japanese references as allegedly suggesting that the use of flip-chip bump connections for coupling an integrated circuit chip to a base was well known. However, none of these references teach or suggest a device as recited in claim 1 in which the base includes a layered part, the lower layered part having a larger opening than the upper layered part. Thus, even if the teachings of the references were to have been combined as in the Office Action, the invention of claim 1 still would not have been achieved.

Moreover, as described in paragraph [0089] of the specification, this design permits the underfill material to properly permeate into the device (i.e., properly permeate to the bonded portion of the bumps), thereby enabling formation of a highly reliable bonding structure. None of the references teach or suggest this advantage of the design, and thus would not have led one of ordinary skill in the art to the device of claim 1 for this additional reason.

Third, regarding claim 22, claim 22 requires that each of the plurality of bumps formed on the semiconductor integrated circuit be shaped to have two levels, a first level having a diameter 0.8 to 0.9 times and a second level having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

The Patent Office has acknowledged that none of the cited references teach or suggest a device having this recited feature. Nevertheless, the Patent Office concluded that such device would have been obvious to one of ordinary skill in the art as derivable through routine trial and error.

Applicant respectfully submits that the Patent Office has failed to establish a prima facie case of obviousness. Specifically, the Patent Office has acknowledged that a recited limitation is absent from the cited art, yet nevertheless concludes, without any basis in the art for doing so, that the limitation would have been obvious as derivable via trial and error. The rejection thus lacks basis, both legally and technically. Even for a limitation to be properly found obvious on the basis of routine optimization, it is still necessary for the art to provide some guidance/suggestion as to the variable to be optimized (i.e., provide a reason that one would explore the variable in the first place). Here, no such basis is provided in the cited art at all. Thus, nothing in the art would have led one to look to the relationship among the dimensions of the layers of a bump as in the invention of claim 22 at all, much less direct one to adjust that relationship and thus possibly arrive at the relationship recited in claim 22.

The only one of the cited references even mentioning layered bumps is JP 540. While JP 540 describes a bump structure comprising two layers, JP 540 does not appear to teach or suggest the dimensions recited in claim 22 for the layers, nor any basis for adjusting the dimensions of the layers with respect to each other and the length of an opening in a pad.

Finally, claims 23, 24 and 29 further recite particular properties of the structure of the device related to an application direction of the ultrasonic waves. None of the art cited by the Patent Office teaches or suggests any of these properties. These claims further distinguish over the teachings of the cited art in the Office Action for this additional reason.

For all the foregoing reasons, Applicant respectfully submits that none of Kondo, Knecht, JP 732, JP 540 or JP 606, whether taken singly or together, teach or suggest the

various claims of the present application. Reconsideration and withdrawal of this rejection are respectfully requested.

B. Kondo or Knecht in View of JP 540 or JP 606 and Further in View of Inoi

Claims 10-13 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Kondo or Knecht in view of JP 540 or JP 606, and further in view of U.S. Patent No. 6,057,633 (Inoi). This rejection is respectfully traversed.

Dependent claim 10 and independent claim 14 recite that at least one side wall of the base facing the side of the semiconductor integrated circuit protrudes into the opening in the base to form a protrusion. As acknowledged by the Patent Office, none of Kondo, Knecht, JP 540 or JP 606 teach or suggest this feature. The Patent Office turned to the teachings of Inoi as allegedly suggesting this feature. Applicant respectfully disagrees.

Inoi describes a piezoelectric transformer unit that includes two casings that snap together to house therein the piezoelectric transforming element. As shown in Figure 11 and described at column 8 of Inoi, the piezoelectric transforming element may include elastic projections thereon so that the unit generates an extremely small amount of noise during operation since the projections prevent the element from directly touching the casing. See column 9, lines 5-9.

Inoi thus describes elastic protrusions attached to the surface of the piezoelectric transformer element. Such does not teach or suggest a side wall of a base facing a semiconductor integrated circuit having protrusions protruding into an opening in the base. The protrusion in claim 10 is formed in a side wall of the base, and is not a protrusion from a surface of the integrated circuit as in Inoi. Inoi thus does not teach or suggest the additional features of claims 10-14 of the present application.

For at least the foregoing reasons, Applicant respectfully submits that none of Kondo, Knecht, JP 540, JP 606 or Inoi would have led one of ordinary skill in the art to the invention of claims 10-13. Reconsideration and withdrawal of this rejection are respectfully requested.

IV. Conclusion

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1-5, 7-24 and 26-32 are in condition for allowance. Should the Examiner believe that anything further is necessary in order to place the application in even better condition, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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JAO:CWB/rxg

Attachments:
Appendix
Copy of Request for Approval of Drawing Corrections

Date: September 17, 2002

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